

Claim Amendments

Please replace the previous claims with the claims listed below.

Claims 1-67 (canceled)

100. (new) A circuit for digital signal processing of multi-sampled phase (DSP MSP) providing measurements and processing of time intervals defining duration of wave-form pulses having frequencies ranging from zero to 1/2 of technology's maximum clock frequency wherein resolution of said intervals measurements matches single gate delays produced by outputs of a delay line built with serially connected gates which a sampling clock is propagated through, wherein the DSP MSP comprises;
- a wave capturing circuit for sampling the incoming wave-form in time instances produced by the outputs of the delay line which the sampling clock is propagated through and for buffering the resulting samples until they are read by a synchronous sequential processor;
- the synchronous sequential processor (SSP) for detecting positioning of leading and trailing edges of the wave-form pulses, and for calculating said time intervals defining duration of wave-form pulses wherein said intervals are measured in numbers of the time instances occurring between the leading and the trailing edges of the pulses, and for processing such having variable lengths intervals in order to perform an analysis of the wave-form or to extract data from the wave-form signal.
101. (new) A DSP MSP as claimed in claim 100 wherein the SSP performs a sequential data recovery (SDR) from the incoming wave-form, wherein the SSP comprises the steps of:
- using an amplitude of a captured wave-form pulse to determine a binary number transmitted during every unit interval defined by transmitter's clock;
- dividing a received pulse duration by a local clock cycle, which is very close to the unit interval, in order to determine how many of said binary numbers need to be assembled into a sequence representing all the data received in the wave-form pulse.

102. (new) A DSP MSP as claimed in claim 101, wherein the SSP comprises:
sequential processing stages configured into a sequential synchronous pipeline driven
synchronously with said sampling clock.

103. (new) A DSP MSP as claimed in claim 102, wherein said sequential processing stages
further comprise:
selectors of input data or arithmometers or output registers.

104. (new) A DSP MSP as claimed in claim 102, wherein the SSP comprises the steps of:
decoding of active edges of the signal;
using the results of the decoding for controlling operations of the next processing stages.

105. (new) A DSP MSP as claimed in claim 102 wherein the SSP performs continues
filtering of the whole incoming wave-form with digital noise filters which filter out
phase noise from wave-form edges or filter out amplitude glitches from wave-form
pulses, wherein the SSP comprises:
a filter mask register providing a pattern which is compared with a captured wave-form of an
input signal;
a filter arithmometer which uses the mask registers content for corrections of captured wave-
forms.

106. (new) A DSP MSP as claimed in claim 105, wherein the SSP comprises:
filter control register which provides code controlling operations of said filter arithmometer in
order to produce said corrections of captured wave-forms.

107. (new) A DSP MSP as claimed in claim 106, further including a programmable control
unit (PCU) for reading results of captured signal processing from the SSP and for controlling
operations of the SSP; wherein the PCU comprises:
means for programming the filter mask register and/or programming the filter control

register, which are applied for achieving said filtering of captured wave-forms.

108. (new) A DSP MSP as claimed in claim 102, further comprising:

multiple said sequential synchronous pipelines configured as parallel processing stages, wherein different said parallel processing stages perform different logical or arithmetical operations during the same phase since the same clock is applied simultaneously to all the parallel stages belonging to the same level of different pipelines.

109. (new) A DSP MSP as claimed in claim 108, comprising merging of said parallel processing stages; wherein:

said multiple parallel processing stages are merged into a smaller number of parallel stages or into a single processing stage, when passing from one said sequential processing stage to the next sequential stage.

110. (new) A DSP MSP as claimed in claim 108, comprising splitting of said parallel processing stages; wherein:

one said processing stage is split into multiple parallel processing stages or multiple parallel processing stages are split into even more parallel stages, when passing from one said sequential processing stage to the next sequential stage.

111. (new) A DSP MSP as claimed in claim 108, wherein:

said sequential processing stages use selectors and/or arithmometers
and/or output registers;

output of said selector which belongs to one parallel processing stage, is used for controlling functions of other selector which belongs to other parallel processing stage.

112. (new) A DSP MSP as claimed in claim 102, wherein:

the SSP comprises parallel processing phases implemented with said synchronous sequential pipelines;

said parallel processing phases are driven by clocks having two or more times lower frequencies than said sampling clock;

consecutive parallel phases are driven by clocks which are shifted in time by one or more

periods of said sampling clock.

113. (new) A DSP MSP as claimed in claim 112, wherein the SSP comprises:
digital noise filters which filter out phase noise from wave-form edges or filter out amplitude
glitches from wave-form pulses, wherein the digital noise filters use multiple noise
filtering sequential stages in every parallel processing phase in order to extend a range
of said wave-form filtering beyond a boundary of a single phase.

114. (new) A DSP MSP as claimed in claim 113, wherein:
carry over bit or bits of an output register of a first filter stage of one phase is or are clocked-
in into an output register of the first filter stage of a next phase together with filtering
results of the next phase;
a second filter stage of the next phase uses the output register of the first filter stage for
filtering a wave-form interval which extends into the next phase.

115. (new) A DSP MSP as claimed in claim 112, comprising merging of said parallel
processing phases; wherein:
multiple said parallel processing phases are merged into a smaller number of parallel phases
or into a single processing phase, when passing from one said sequential processing
stage to the next sequential stage.

116. (new) A DSP MSP as claimed in claim 112 comprising splitting of said parallel
processing phases, wherein:
one said processing phase is split into multiple parallel processing phases or multiple parallel
processing phases are split into even more parallel phases, when passing from one
said sequential processing stage to the next sequential stage.

117. (new) A DSP MSP as claimed in claim 112, comprising time sharing of said parallel
processing phases; wherein:
a task of processing of a newly captured wave-form edge or a newly began wave-form pulse,
is assigned to a next available parallel processing phase.

118. (new) A DSP MSP as claimed in claim 112, comprising the steps of:
passing outputs of one said parallel processing phase to the next parallel phase.

using said passed outputs for processing conducted by a sequential processing stage which belongs to the next parallel processing phase.

119. (new) A DSP MSP as claimed in claim 118, further comprising the step of: re-timing output register bits of the original parallel phase, by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase.

120. (new) A DSP MSP as claimed in claim 102, wherein:
an active edge of the wave-form is detected by capturing a change in a wave-form level by one of the sub-clocks;
said edge capturing sub-clock defines an edge skew between an edge of the sampling clock and the wave-form edge;
pulse duration is composed of said edge skew of a front edge of the incoming wave-form, and an integer number of sampling clock periods between the front edge and an end edge, and said edge skew of the end edge of the wave-form.

121. (new) A DSP MSP as claimed in claim 102 wherein said SSP enables real-time processing of densely over-sampled signal reaching $1/2$ of technology's maximum clock frequency, wherein a complex signal processing operation including said division of the pulse duration conventionally requiring whole input argument to be available before processing it with a single processing stage used repeatedly through multiple micro-cycles, is now performed when the input argument keeps still coming in while it is processed with serially connected processing stages dedicated to particular singular micro-cycles, wherein the SSP comprises:
the first sequential processing stage which is connected to outputs of the wave-form capture circuit and the remaining stages which are pipe-lined in accordance with the timing of their operations, wherein the sequential stages are clocked by the sampling clock sub-clocks;
means for performing every consecutive micro-cycle of the complex operation by the separate dedicated processing stage during an assigned time slot synchronous with the

sampling clock providing a fundamental timing for the whole signal processing operation wherein said operation keeps progressing while its argument still keeps coming in, wherein data sampled during a time interval equal to the assigned time slot is passed only ones through an arithmometer of every micro-cycle's dedicated stage when the processed data stream is moving down the SSP.

122. (new) A DSP MSP as claimed in claim 102 including a fractional bit staffing method (FBS) for increasing speed of said division of the received pulse duration wherein the FBS allows indefinitely long dividers enabling accuracy better than sampling digitization error; wherein the FBS:

defines the local clock cycle as the divider consisting of an integer part representing an integer number of said sampling time instances and a fractional part representing a fraction of the sampling time instance, wherein the fractional part is defined as a series of binary terms;

produces a first component of division result and a remainder by subtracting the integer part from the pulse duration;

produces a second component of division result and a new remainder by subtracting the integer part and the first term of the series from the previous step remainder if the previous remainder was positive, or terminates the division if the previous remainder was negative or zero;

and similarly produces an n component of division result and a new remainder by subtracting the integer part and the $n-1$ term of the series from the previous step remainder if the previous remainder was positive, or terminates the division if the previous remainder was negative or zero.

123. (new) A DSP MSP as claimed in claim 122, wherein:

said series of binary terms is downloaded to a register;

a circuit which performs said division operation, uses said terms by shifting the register during any operation and accessing the same portion of the register or by using a selector circuit which selects a consecutive portion of the register which contains the

corresponding terms.

124. (new) A DSP MSP as claimed in claim 102, comprising a periodical skew accumulation method (PSA); wherein the PSA:
- calculates an estimate of the unit interval produced by the transmitter's clock based on processing of said measured time intervals defining pulses duration;
 - calculates a periodical skew as a difference between the estimate of the unit interval and the local clock cycle, wherein the periodical skew comprises an integer part representing an integer number of said sampling time instances and a fractional part representing a fraction of the sampling time instance wherein the fractional part is defined as a series of binary terms;
 - modifies a dividers integer for said dividing of received pulse duration by adding the integer part of the periodical skew to an integer part of the local clock cycle;
 - modifies a dividers fractional part for said dividing of received pulse duration by adding the binary terms of the fractional part of the periodical skew to corresponding binary terms of a fractional part of the local clock cycle, wherein the resulting dividers fractional part is defined as a series of binary terms as well;
 - produces a first digit of division result and a remainder by subtracting the modified divider integer from the pulse duration;
 - produces a second digit of division result and a new remainder by subtracting the modified integer and the first term of the modified fractional part from the previous step remainder if the previous remainder was positive, or terminates the division if the previous remainder was negative or zero;
 - and similarly produces an n digit of division result and a new remainder by subtracting the modified divider integer and the n-1 term of the modified fractional part from the previous step remainder if the previous remainder was positive, or terminates the division if the previous remainder was negative or zero.
125. (new) A DSP MSP as claimed in claim 124, wherein the PSA comprises:
- downloading said series of binary terms to a register;

providing said terms to a circuit which performs said division operation, by shifting the register during any operation and accessing the same portion of the register or by using a selector circuit which selects a consecutive portion of the register which contains the corresponding terms.

126. (new) A DSP MSP as claimed in claim 102, comprising a periodical skew accumulation method (PSA); wherein the PSA:
calculates an estimate of the unit interval produced by the transmitter's clock based on processing of said measured time intervals defining pulses duration;
calculates a periodical skew as a difference between the estimate of the unit interval and the presently used local clock cycle, wherein the periodical skew comprises an integer part representing an integer number of said sampling time instances and a fractional part representing a fraction of the sampling time instance wherein the fractional part is defined as a series of binary terms;
calculates accumulations of said periodical skews during a received pulse of the incoming signal, wherein the integer part of the periodical skew is accumulated at any consecutive expiration of the local clock cycle and an $n-1$ term of the series is accumulated at an n expiration of the local clock cycle;
adds resulting total accumulation to the measured pulse duration before performing said dividing of said received pulse duration.
127. (new) A DSP MSP as claimed in claim 108 comprising a received data collection circuit (RDC) for recovering and registering data from samples provided by the wave capturing circuit; wherein:
the RDC uses the parallel processing stages for collecting data which is recovered by other parallel processing stages from the wave-form pulse which is still incoming and is still processed by said other parallel processing stages performing said data recovery.
128. (new) A DSP MSP as claimed in claim 112 comprising a received data collection circuit (RDC) for recovering and registering data from samples provided by the wave

capturing circuit; wherein:

the RDC uses the parallel processing phase for collecting data which is recovered by other parallel processing phase from the wave-form pulse which is still coming in and is still processed by said other parallel processing phase performing said data recovery.

129. (new) A DSP MSP as claimed in claim 102, comprising a data frequency capturing circuit (DFC) for recovering and capturing a frequency of the transmitter's clock of said captured wave-form; wherein the DFC comprises:

means for defining expected time intervals for data patterns recovered from the incoming wave-form pulses, based on current estimate of the unit interval;

means for using the expected time intervals and the detected time intervals, for estimating frequency of the incoming wave-form clock versus the local clock frequency;

or means for using a difference between said expected time intervals and said detected time intervals, for a frequency estimation of the incoming wave-form clock versus the local clock.

130. (new) A DSP MSP as claimed in claim 129; wherein the DFC comprises:

means for accumulating total detected time interval of any indefinite continues sequence of wave-form pulses without any accumulation of digitization errors inevitably accompanying detection of edges of any specific wave-form pulse;

whereby the digitization error of the total detected interval remains smaller than said sampling instances resolution independently of number of pulses contained in the continues sequence.

131. (new) A DSP MSP as claimed in claim 102 comprising a wave-form screening and capturing circuit (WFSC) for verifying if the incoming wave-form captured with the resolution matching single gate delays is compliant with programmable patterns; wherein the WFSC comprises:

means for using programmable screening masks and/or programmable control codes for verifying incoming wave-form captures for compliance with said programmable

screening patterns.

132. (new) A DSP MSP as claimed in claim 131, wherein the WFSC comprises:
means for buffering captured wave-form for which the pre-programmed compliance or non-compliance has been detected, or for counting a number of said detections;
means for communicating said buffered wave-form and/or a detections counter, to an internal control circuit and/or to an external unit.

133. (new) A DSP MSP as claimed in claim 132, further including a programmable control unit (PCU) for reading results of captured signal processing from the WFSC and for controlling operations of the WFSC; wherein the PCU comprises:
means for programming the screening masks and/or the control codes for performing said verification of captured wave-forms compliance or non-compliance with said screening patterns;
means for reading verification results and/or reading captured wave-forms which correspond to the preprogrammed verification criteria.

134. (new) A DSP MSP as claimed in claim 131, wherein the WFSC comprises:
means for using programmable time slot selection circuits for selecting a time interval of incoming wave-form;
means for buffering said incoming wave-form captured during the selected time interval and for communicating such buffered wave-form to an internal control circuit and/or to an external unit.

135. (new) A DSP MSP as claimed in claim 134, further including a programmable control unit (PCU) for reading results of captured signal processing from the WFSC and for controlling operations of the WFSC; wherein the PCU comprises:
means for programming said slot selections performed by the WFSC;
means for reading and analyzing said buffered wave-forms.

136. (new) A DSP MSP as claimed in claim 102, further including a programmable control unit (PCU) for controlling operations of the SSP; wherein:
the PCU is connected to the SSP and reads status of said SSP processing stages;
the PCU provides arguments for operations performed by said processing stages or control codes defining functions performed by the processing stages.
137. (new) A synchronous sequential processor (SSP) multiplying processing throughput for enabling real-time processing of densely over-sampled signal reaching $1/2$ of technology's maximum clock frequency, wherein a complex signal processing operation such as division or multiplication or digital integration previously requiring whole input argument to be available before processing it with a single processing stage used repeatedly through multiple micro-cycles, is now performed while the input argument still keeps coming in when it is processed with serially connected processing stages dedicated to particular singular micro-cycles; the SSP comprising:
a delay line of a sampling clock, which is built with serially connected gates producing sub-clocks representing variety of phase displacements of the sampling clock;
a wave-form capture circuit using said sub-clocks to sample and to capture instantaneous amplitudes of the input signal;
the first sequential processing stage which is connected to outputs of the wave-form capture circuit and the remaining stages which are pipe-lined in accordance with the timing of their operations, wherein the sequential stages are clocked by the sampling clock sub-clocks;
means for performing every consecutive micro-cycle of the complex operation by the separate dedicated processing stage during an assigned time slot synchronous with the sampling clock providing a fundamental timing for the whole signal processing operation wherein said operation keeps progressing while its argument still keeps coming in, wherein data sampled during a time interval equal to the assigned time slot is passed only ones through an arithmometer of every micro-cycle's dedicated stage when the processed data stream is moving down the SSP.

138. (new) A DSP MSP as claimed in claim 102 including the wave capturing circuit further comprising a sequential clocks generator (SCG) which enables selective use of very close sub-clocks produced by serially connected gates of the delay line of the sampling clock wherein entire sets of sub-clocks occurring during different periodically interleaving cycles of the sampling clock are selected first and such specific sets further named phases enable further selection of single sub-clocks; the DSP MSP wherein the SCG comprises:

sub-clocks phase selectors which are serially connected in the opposite order than their sub-clocks and the phase selector of the last sub-clock has its input connected to its own output while every phase selector of any other sub-clock is connected to the output of the phase selector of the next sub-clock, wherein the phase selectors use flip-flops switched by falling edges of the sub-clocks for performing said phase selections if said phases consist of positive sub-clocks or use flip-flops switched by rising edges of the sub-clocks for performing said phase selections if said phases consist of negative sub-clocks;

means for using such different phases of sub-clocks for capturing consecutive intervals of the incoming wave-form in different registers, in order to avoid overwriting of already captured data before it is moved down into the SSP;

means for further selection of single sub-clocks from particular phases, in order to provide sub-clocks defining time slots assigned for particular stages of the SSP.

139 (new) A sequential clocks generator (SCG) enabling selective use of very close sub-clocks produced by serially connected gates of a delay line of a sampling clock wherein whole sets of sub-clocks occurring during different periodically interleaving cycles of the sampling clock are selected first and such specific sets further named phases enable further selection of single sub-clocks, the SCG comprising:

the delay line of the sampling clock built with serially connected gates producing the sub-clocks;

sub-clocks phase selectors for enabling the sub-clocks during said phases wherein the sub-clocks phase selectors are serially connected in the opposite order than their sub-

clocks and the phase selector of the last sub-clock has its input connected to its own output while every phase selector of any other sub-clock is connected to the output of the phase selector of the next sub-clock, wherein the phase selectors use flip-flops switched by falling edges of the sub-clocks for performing said phase selections if said phases consist of positive sub-clocks or use flip-flops switched by rising edges of the sub-clocks for performing said phase selections if said phases consist of negative sub-clocks.

140. (new) A fractional bit staffing method (FBS) for multiplying speed of complex division operation involving use of a fixed divider for processing a changing data stream wherein the FBS allows indefinitely long dividers enabling accuracy better than least significant bit of the processed data; wherein the FBS comprises the steps of:
- using said divider consisting of a fixed integer part and a fractional part representing a fraction of the least significant bit of a dividend wherein the fractional part is defined as a series of binary terms;
- producing a first component of division result and a remainder by subtracting the integer part from the processed number from said data stream;
- producing a second component of division result and a new remainder by subtracting the integer part and the first term of the series from the previous step remainder if the previous remainder was positive, or terminating the division if the previous remainder was negative or zero;
- and similarly producing an n component of division result and a new remainder by subtracting the integer part and the n-1 term of the series from the previous step remainder if the previous remainder was positive, or terminating the division if the previous remainder was negative or zero.
141. (new) A circuit for digital signal processing of multi-sampled phase (DSP MSP) providing measurements and processing of time intervals defining duration of waveform pulses having frequencies ranging from zero to 1/2 of technology's maximum

clock frequency wherein resolution of said intervals measurements matches single gate delays produced by outputs of a delay line built with serially connected gates which a sampling clock or said wave-form is propagated through, wherein the DSP MSP comprises:

- a wave capturing circuit for sampling the incoming wave-form in time instances produced by the outputs of the delay line which the sampling clock or the wave-form is propagated through and for buffering the resulting samples until they are read by a phase processing unit;
- the phase processing unit for detecting positioning of leading and trailing edges of the wave-form pulses, and for calculating said time intervals defining duration of wave-form pulses wherein said intervals are measured in numbers of the time instances occurring between the leading and the trailing edges of the pulses, and for processing such having variable lengths intervals in order to perform an analysis of the wave-form or to extract data from the wave-form signal.

142. (new) A DSP MSP as claimed in claim 141 wherein the SSP performs a sequential data recovery (SDR) from the incoming wave-form, wherein the SSP comprises the steps of:

- using an amplitude of a captured wave-form pulse to determine a binary number transmitted during every unit interval defined by transmitter's clock;
- dividing a received pulse duration by a local clock cycle, which is very close to the unit interval, in order to determine how many of said binary numbers need to be collected into a sequence representing all the data received in the wave-form pulse.